SOJ, TSOP, FP-BGA, TQFP
Commercial Temp
Industrial Temp

128K x 16
2Mb Asynchronous SRAM

7, 8, 10, 12 ns
3.3 V V_{DD}
Center V_{DD} and V_{SS}

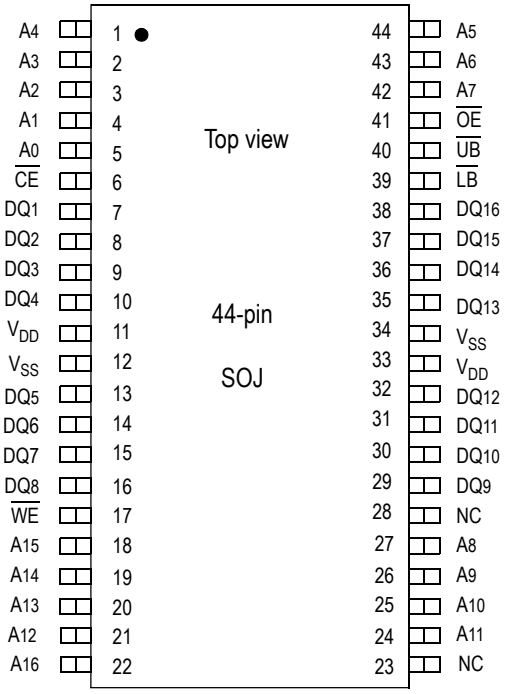
Features

- Fast access time: 7, 8, 10, 12 ns
- CMOS low power operation: 145/125/100/85 mA at minimum cycle time
- Single 3.3 V power supply
- All inputs and outputs are TTL-compatible
- Byte control
- Fully static operation
- Industrial Temperature Option: –40° to 85°C
- Package line up
  - J: 400 mil, 44-pin SOJ package
  - TP: 400 mil, 44-pin TSOP Type II package
  - T: 10 mm x 10 mm, 44-pin TQFP
  - U: 6 mm x 8 mm Fine Pitch Ball Grid Array package

Description

The GS72116A is a high speed CMOS Static RAM organized as 131,072 words by 16 bits. Static design eliminates the need for external clocks or timing strobes. The GS operates on a single 3.3 V power supply and all inputs and outputs are TTL-compatible. The GS72116A is available in a 6 mm x 8 mm Fine Pitch BGA package, a 10 mm x 10 mm TQFP package, as well as in 400 mil SOJ and 400 mil TSOP Type-II packages.

SOJ 128K x 16-Pin Configuration

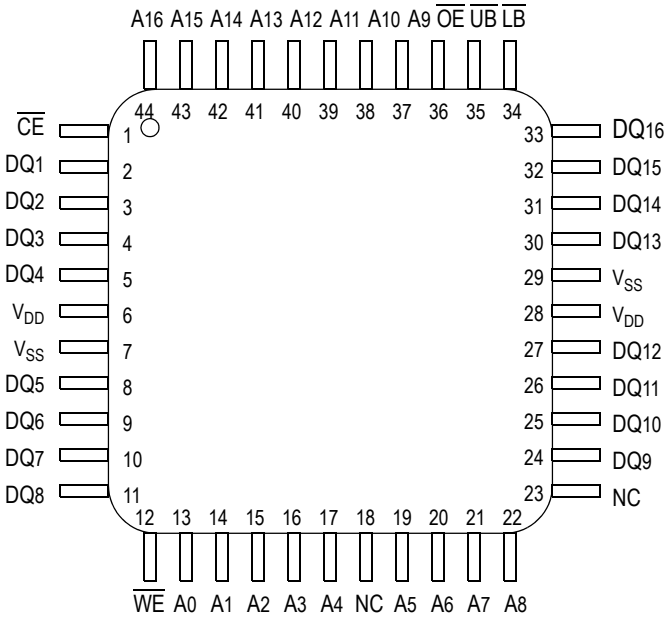


Package J

Pin Descriptions

Symbol	Description
A_0–A_{16}	Address input
DQ_1–DQ_{16}	Data input/output
$\overline{CE}$	Chip enable input
$\overline{LB}$	Lower byte enable input (DQ1 to DQ8)
$\overline{UB}$	Upper byte enable input (DQ9 to DQ16)
$\overline{WE}$	Write enable input
$\overline{OE}$	Output enable input
V_{DD}	+3.3 V power supply
V_{SS}	Ground
NC	No connect

44-Pin TQFP 128K x 16-Pin Configuration



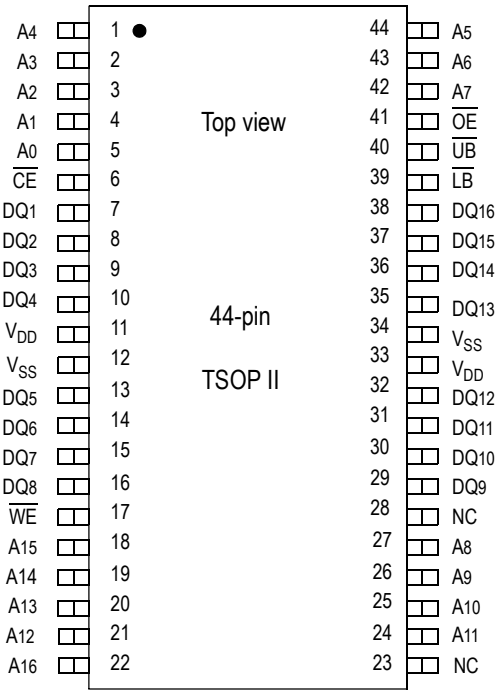
Package T

Fine Pitch BGA 128K x 16-Bump Configuration

	1	2	3	4	5	6
A	$\overline{LB}$	$\overline{OE}$	A0	A1	A2	NC
B	DQ16	$\overline{UB}$	A3	A4	$\overline{CE}$	DQ1
C	DQ14	DQ15	A5	A6	DQ2	DQ3
D	V_{SS}	DQ13	NC	A7	DQ4	V_{DD}
E	V_{DD}	DQ12	NC	A16	DQ5	V_{SS}
F	DQ11	DQ10	A8	A9	DQ7	DQ6
G	DQ9	NC	A10	A11	$\overline{WE}$	DQ8
H	NC	A12	A13	A14	A15	NC

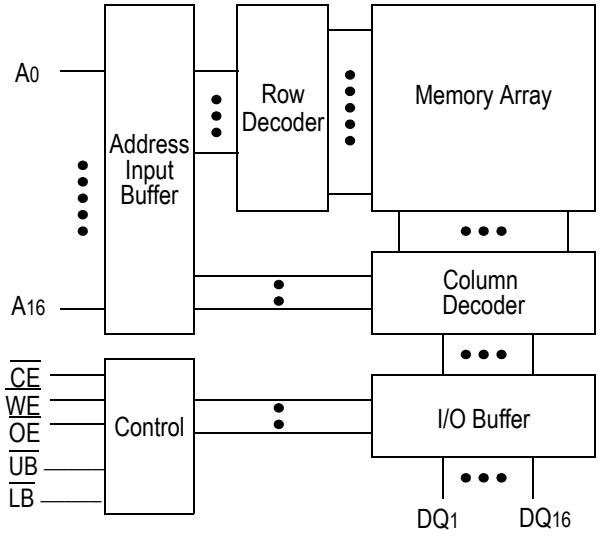
6 mm x 8 mm, 0.75 mm Bump Pitch
Top View
Package U

TSOP-II 128K x 16-Pin Configuration



Package TP

Block Diagram



Truth Table

$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	$\overline{LB}$	$\overline{UB}$	DQ1 to DQ8	DQ9 to DQ16	VDD Current
H	X	X	X	X	Not Selected	Not Selected	ISB1, ISB2
L	L	H	L	L	Read	Read	IDD
			L	H	Read	High Z	
			H	L	High Z	Read	
L	X	L	L	L	Write	Write	
			L	H	Write	Not Write, High Z	
			H	L	Not Write, High Z	Write	
L	H	H	X	X	High Z	High Z	
L	X	X	H	H	High Z	High Z	

Note: X: "H" or "L"

Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
Supply Voltage	V_{DD}	–0.5 to +4.6	V
Input Voltage	V_{IN}	–0.5 to V_{DD} +0.5 (≤ 4.6 V max.)	V
Output Voltage	V_{OUT}	–0.5 to V_{DD} +0.5 (≤ 4.6 V max.)	V
Allowable power dissipation	PD	0.7	W
Storage temperature	T_{STG}	–55 to 150	°C

Note:
Permanent device damage may occur if Absolute Maximum Ratings are exceeded. Functional operation shall be restricted to Recommended Operating Conditions. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage for -7/-8/-10/12	V_{DD}	3.0	3.3	3.6	V
Input High Voltage	V_{IH}	2.0	—	V_{DD} +0.3	V
Input Low Voltage	V_{IL}	–0.3	—	0.8	V
Ambient Temperature, Commercial Range	T_{Ac}	0	—	70	°C
Ambient Temperature, Industrial Range	T_{AI}	–40	—	85	°C

Note:
1. Input overshoot voltage should be less than V_{DD} +2 V and not exceed 20 ns.
2. Input undershoot voltage should be greater than –2 V and not exceed 20 ns.

Capacitance

Parameter	Symbol	Test Condition	Max	Unit
Input Capacitance	C_{IN}	V_{IN} = 0 V	5	pF
Output Capacitance	C_{OUT}	V_{OUT} = 0 V	7	pF

Notes:
1. Tested at T_A = 25°C, f = 1 MHz
2. These parameters are sampled and are not 100% tested.

DC I/O Pin Characteristics

Parameter	Symbol	Test Conditions	Min	Max
Input Leakage Current	I_{IL}	V_{IN} = 0 to V_{DD}	– 1 uA	1 uA
Output Leakage Current	I_{LO}	Output High Z V_{OUT} = 0 to V_{DD}	–1 uA	1 uA
Output High Voltage	V_{OH}	I_{OH} = –4mA	2.4	—
Output Low Voltage	V_{OL}	I_{LO} = +4mA	—	0.4 V

Power Supply Currents

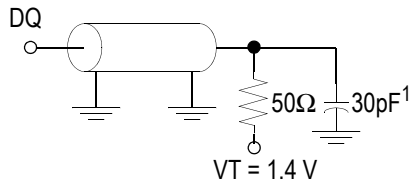
Parameter	Symbol	Test Conditions	0 to 70°C				–40 to 85°C			
			7 ns	8 ns	10 ns	12 ns	7 ns	8 ns	10 ns	12 ns
Operating Supply Current	IDD (max)	$\overline{CE} \leq$ VIL All other inputs ≥ VIH or ≤ VIL Min. cycle time IOUT = 0 mA	145 mA	125 mA	100 mA	85 mA	150 mA	130 mA	105 mA	90 mA
Standby Current	ISB1 (max)	$\overline{CE} \geq$ VIH All other inputs ≥ VIH or ≤VIL Min. cycle time	25 mA	20 mA	20 mA	15 mA	30 mA	25 mA	25 mA	20 mA
Standby Current	ISB2 (max)	$\overline{CE} \geq V_{DD} - 0.2$ V All other inputs ≥ $V_{DD} - 0.2$ V or ≤ 0.2 V	5 mA				10 mA			

AC Test Conditions

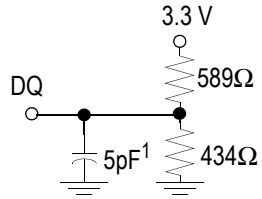
Parameter	Conditions
Input high level	V_{IH} = 2.4 V
Input low level	V_{IL} = 0.4 V
Input rise time	tr = 1 V/ns
Input fall time	tf = 1 V/ns
Input reference level	1.4 V
Output reference level	1.4 V
Output load	**Fig. 1& 2**

Note:
1. Include scope and jig capacitance.
2. Test conditions as specified with output loading as shown in **Fig. 1** unless otherwise noted.
3. Output load 2 for t_{LZ}, t_{HZ}, t_{OLZ} and t_{OHZ}

Output Load 1



Output Load 2



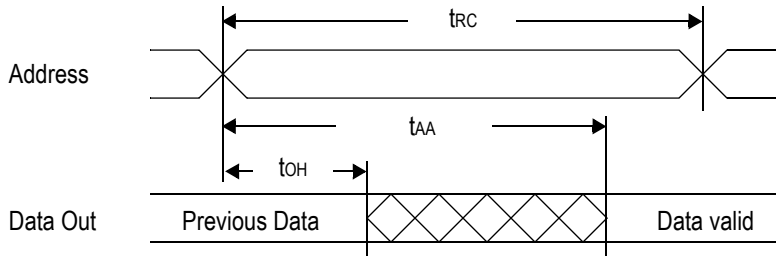
AC Characteristics

Read Cycle

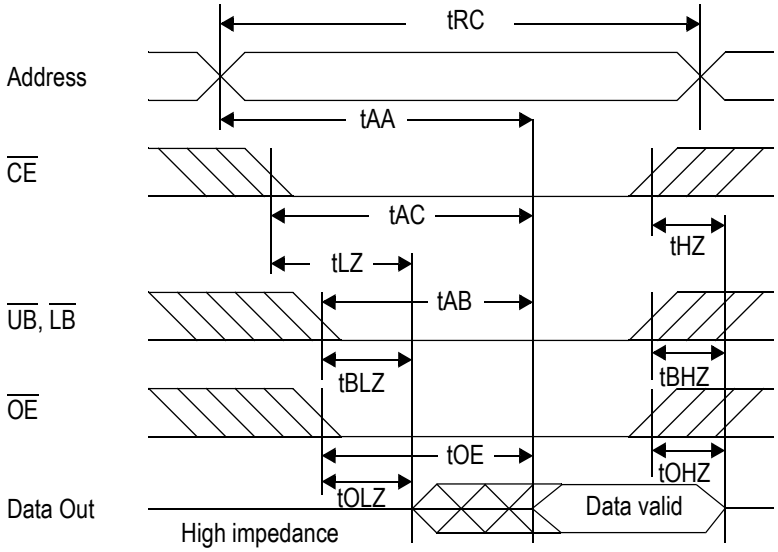
Parameter	Symbol	-7		-8		-10		-12		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
Read cycle time	t_{RC}	7	—	8	—	10	—	12	—	ns
Address access time	t_{AA}	—	7	—	8	—	10	—	12	ns
Chip enable access time ($\overline{CE}$)	t_{AC}	—	7	—	8	—	10	—	12	ns
Byte enable access time ($\overline{UB}$, $\overline{LB}$)	t_{AB}	—	3	—	3.5	—	4	—	5	ns
Output enable to output valid ($\overline{OE}$)	t_{OE}	—	3	—	3.5	—	4	—	5	ns
Output hold from address change	t_{OH}	3	—	3	—	3	—	3	—	ns
Chip enable to output in low Z ($\overline{CE}$)	t_{LZ}*	3	—	3	—	3	—	3	—	ns
Output enable to output in low Z ($\overline{OE}$)	t_{OLZ}*	0	—	0	—	0	—	0	—	ns
Byte enable to output in low Z ($\overline{UB}$, $\overline{LB}$)	t_{BLZ}*	0	—	0	—	0	—	0	—	ns
Chip disable to output in High Z ($\overline{CE}$)	t_{HZ}*	—	3.5	—	4	—	5	—	6	ns
Output disable to output in High Z ($\overline{OE}$)	t_{OHZ}*	—	3	—	3.5	—	4	—	5	ns
Byte disable to output in High Z ($\overline{UB}$, $\overline{LB}$)	t_{BHZ}*	—	3	—	3.5	—	4	—	5	ns

* These parameters are sampled and are not 100% tested.

Read Cycle 1: $\overline{CE}$ = $\overline{OE}$ = V_{IL}, $\overline{WE}$ = V_{IH}, $\overline{UB}$ and, or $\overline{LB}$ = V_{IL}



Read Cycle 2: $\overline{WE}$ = V_{IH}

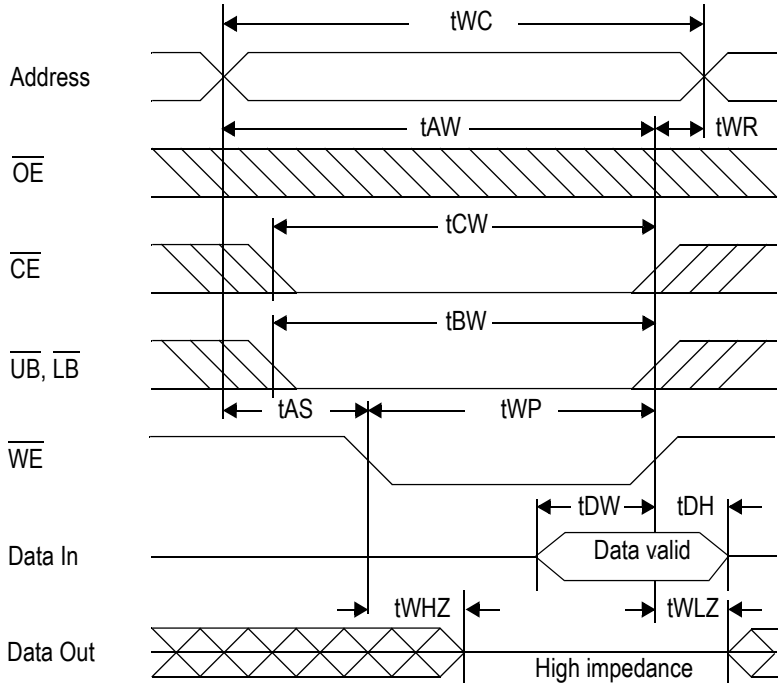


Write Cycle

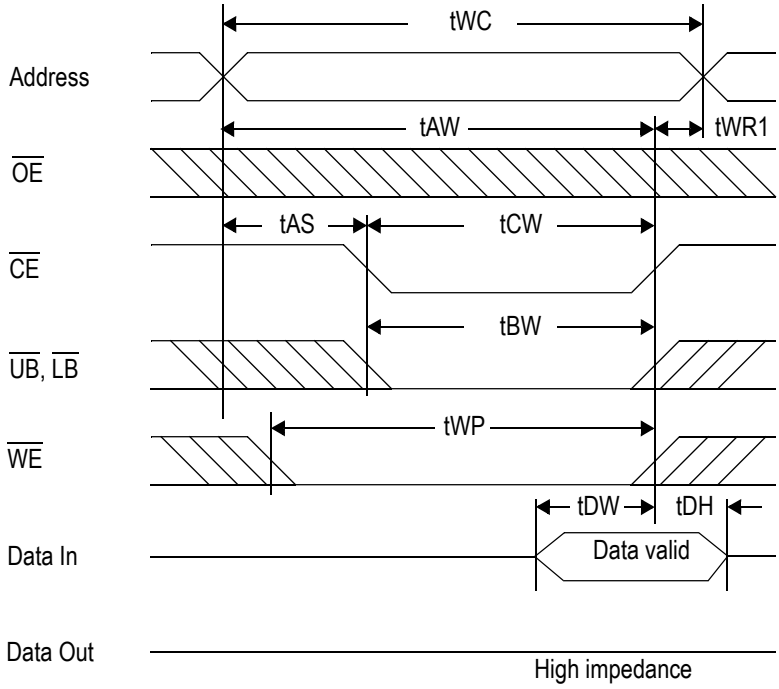
Parameter	Symbol	-7		-8		-10		-12		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
Write cycle time	tWC	7	—	8	—	10	—	12	—	ns
Address valid to end of write	tAW	5	—	5.5	—	7	—	8	—	ns
Chip enable to end of write	tCW	5	—	5.5	—	7	—	8	—	ns
Byte enable to end of write	tBW	5	—	5.5	—	7	—	8	—	ns
Data set up time	tDW	3.5	—	4	—	5	—	6	—	ns
Data hold time	tDH	0	—	0	—	0	—	0	—	ns
Write pulse width	tWP	5	—	5.5	—	7	—	8	—	ns
Address set up time	tAS	0	—	0	—	0	—	0	—	ns
Write recovery time ($\overline{WE}$)	tWR	0	—	0	—	0	—	0	—	ns
Write recovery time ($\overline{CE}$)	tWR1	0	—	0	—	0	—	0	—	ns
Output Low Z from end of write	tWLZ*	3	—	3	—	3	—	3	—	ns
Write to output in High Z	tWHZ*	—	3	—	3.5	—	4	—	5	ns

* These parameters are sampled and are not 100% tested.

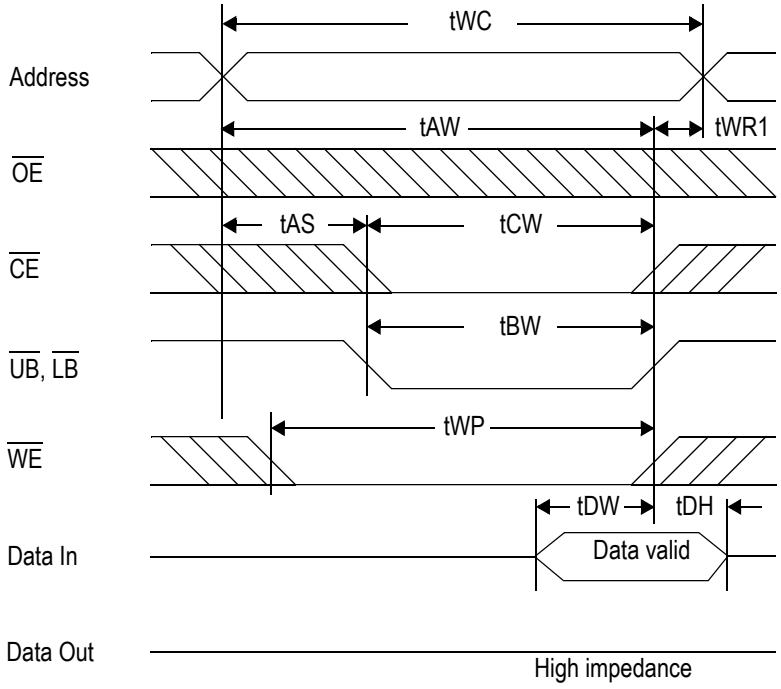
Write Cycle 1: $\overline{WE}$ control



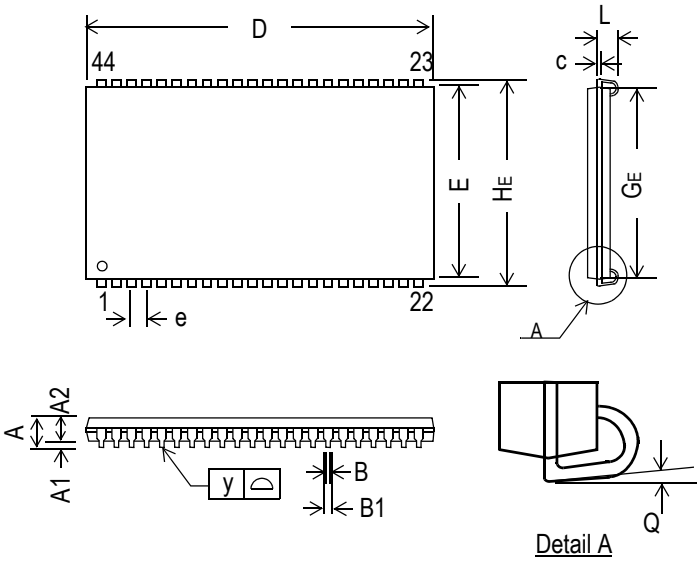
Write Cycle 2: $\overline{CE}$ control



Write Cycle 3: $\overline{UB}$, $\overline{LB}$ control



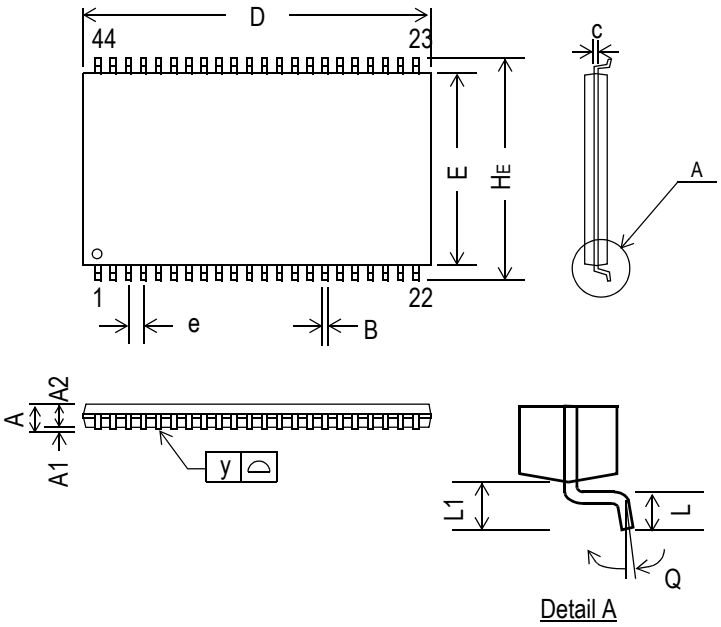
44-Pin, 400 mil SOJ



Symbol	Dimension in inch			Dimension in mm		
	min	nom	max	min	nom	max
A	—	—	0.148	—	—	3.759
A1	0.025	—	—	0.635	—	—
A2	0.105	0.110	0.115	2.667	2.794	2.921
B	—	0.018	—	—	0.457	—
B1	0.026	0.028	0.032	0.660	0.711	0.813
c	—	0.008	—	—	0.203	—
D	1.120	1.125	1.130	28.44	28.58	28.70
E	0.395	0.400	0.405	10.033	10.160	10.287
e	—	0.05	—	—	1.27	—
H_E	0.435	0.440	0.445	11.049	11.176	11.303
G_E	0.360	0.370	0.380	9.144	9.398	9.652
L	0.082	0.087	0.106	2.083	2.210	2.70
y	—	—	0.004	—	—	0.102
Q	0^o	—	7^o	0^o	—	7^o

Note:
1. Dimension D& E do not include interlead flash.
2. Dimension B1 does not include dambar protrusion/intrusion.
3. Controlling dimension: inches

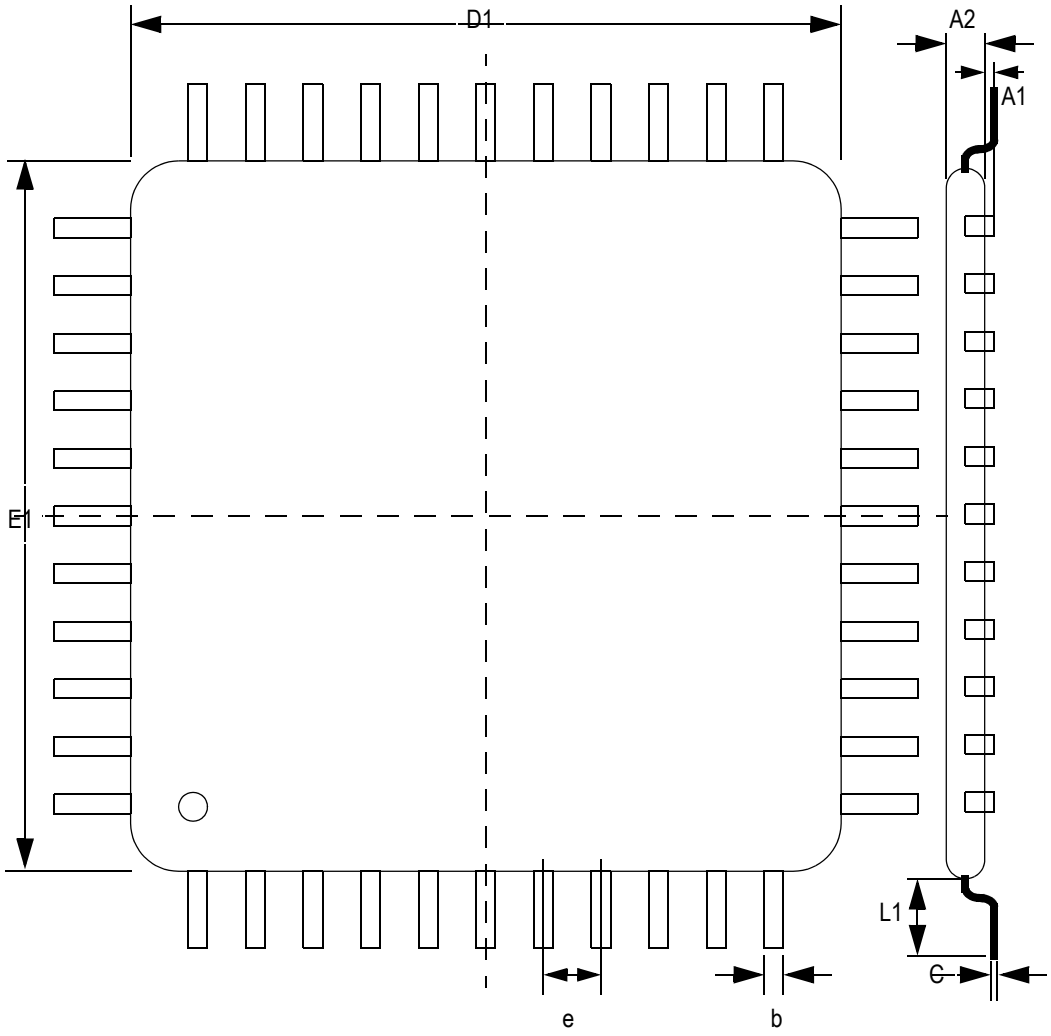
44-Pin, 400 mil TSOP-II



Symbol	Dimension in inch			Dimension in mm		
	min	nom	max	min	nom	max
A	—	—	0.047	—	—	1.20
A1	0.002	—	—	0.05	—	—
A2	0.037	0.039	0.041	0.95	1.00	1.05
B	0.01	0.014	0.018	0.25	0.35	0.45
c	—	0.006	—	—	0.15	—
D	0.721	0.725	0.729	18.31	18.41	18.51
E	0.396	0.400	0.404	10.06	10.16	10.26
e	—	0.031	—	—	0.80	—
H_E	0.455	0.463	0.471	11.56	11.76	11.96
L	0.016	0.020	0.024	0.40	0.50	0.60
L1	—	0.031	—	—	0.80	—
y	—	—	0.004	—	—	0.10
Q	0^o	—	5^o	0^o	—	5^o

Note:
1. Dimension D& E do not include interlead flash.
2. Dimension B does not include dambar protrusion/intrusion.
3. Controlling dimension: mm

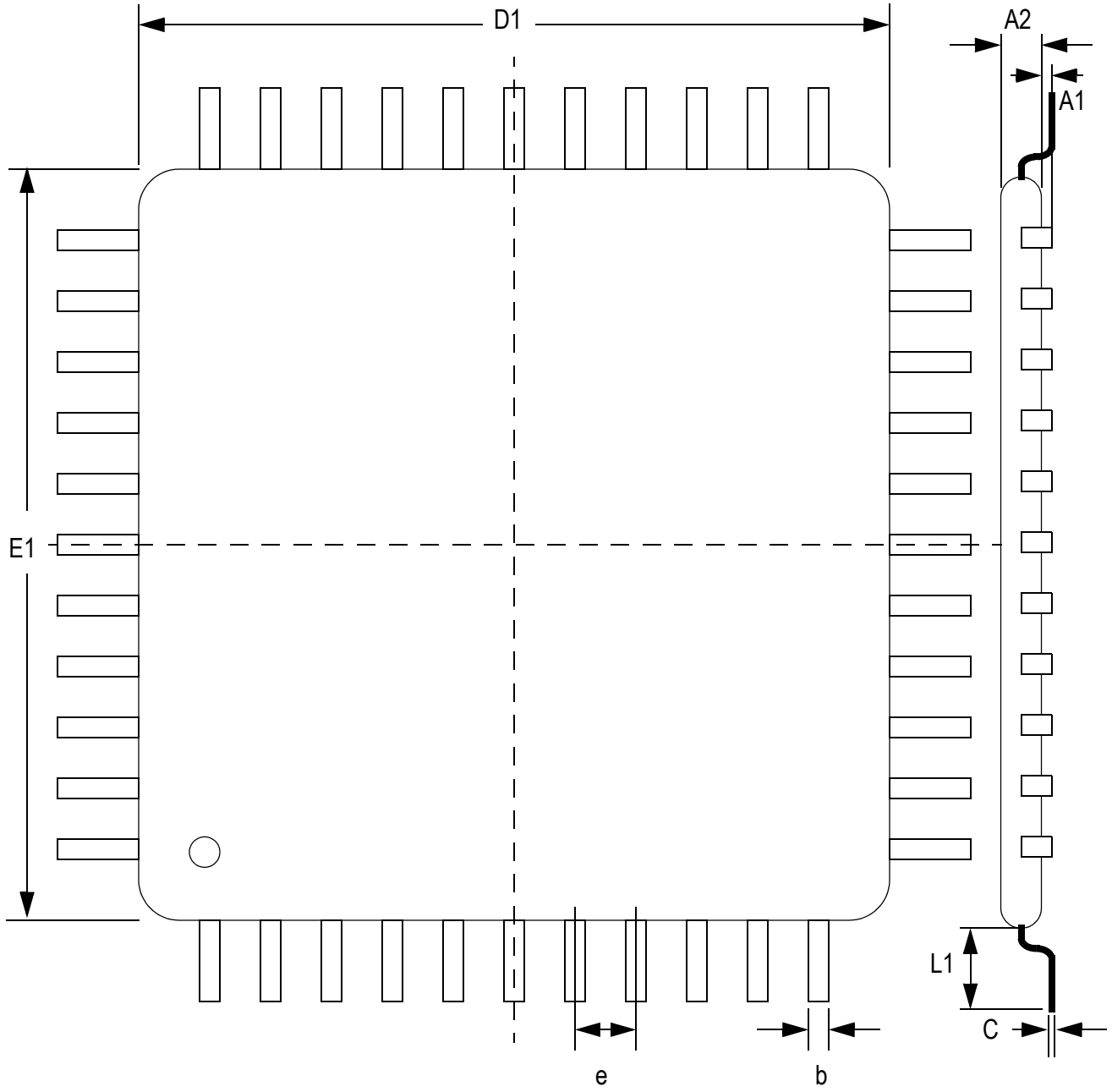
44-Pin TQFP (LQFP) Package



Body Size		Lead Count	Standoff	Body Thickness	Lead Length	Lead Width	Lead Thickness	Lead Pitch
E1	D1		A1	A2	L1	b	c	e
10	10	44	0.1	1.4	1.0	0.3	0.127	0.8

Units: mm

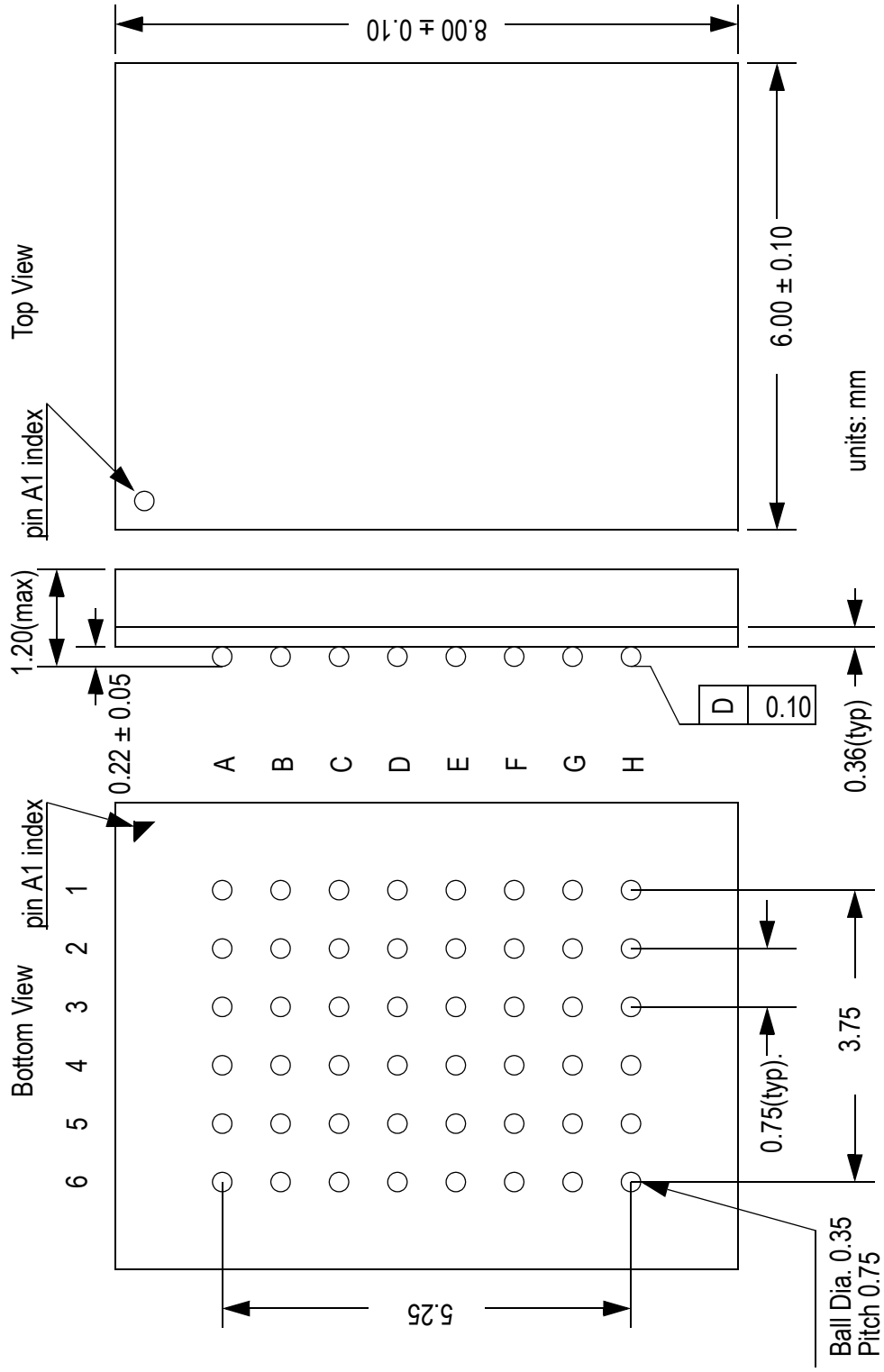
44 Pin TQFP (LQFP) Package



Body Size		Lead Count	Standoff	Body Thickness	Lead Length	Lead Width	Lead Thickness	Lead Pitch
E1	D1		A1	A2	L1	b	c	e
10	10	44	0.1	1.4	1.0	0.3	0.127	0.8

Units: mm

6 mm x 8 mm Fine Pitch BGA



Ordering Information

Part Number*	Package	Access Time	Temp. Range	Status
GS72116ATP-7	400 mil TSOP-II	7 ns	Commercial	
GS72116ATP-8	400 mil TSOP-II	8 ns	Commercial	
GS72116ATP-10	400 mil TSOP-II	10 ns	Commercial	
GS72116ATP-12	400 mil TSOP-II	12 ns	Commercial	
GS72116ATP-7I	400 mil TSOP-II	7 ns	Industrial	
GS72116ATP-8I	400 mil TSOP-II	8 ns	Industrial	
GS72116ATP-10I	400 mil TSOP-II	10 ns	Industrial	
GS72116ATP-12I	400 mil TSOP-II	12 ns	Industrial	
GS72116AJ-7	400 mil SOJ	7 ns	Commercial	
GS72116AJ-8	400 mil SOJ	8 ns	Commercial	
GS72116AJ-10	400 mil SOJ	10 ns	Commercial	
GS72116AJ-12	400 mil SOJ	12 ns	Commercial	
GS72116AJ-7I	400 mil SOJ	7 ns	Industrial	
GS72116AJ-8I	400 mil SOJ	8 ns	Industrial	
GS72116AJ-10I	400 mil SOJ	10 ns	Industrial	
GS72116AJ-12I	400 mil SOJ	12 ns	Industrial	
GS72116AT-7	44-pin TQFP	7 ns	Commercial	
GS72116AT-8	44-pin TQFP	8 ns	Commercial	
GS72116AT-10	44-pin TQFP	10 ns	Commercial	
GS72116AT-12	44-pin TQFP	12 ns	Commercial	
GS72116AT-7I	44-pin TQFP	7 ns	Industrial	
GS72116AT-8I	44-pin TQFP	8 ns	Industrial	
GS72116AT-10I	44-pin TQFP	10 ns	Industrial	
GS72116AT-12I	44-pin TQFP	12 ns	Industrial	

Ordering Information

Part Number*	Package	Access Time	Temp. Range	Status
GS72116AU-7	6 mm x 8 mm Fine Pitch BGA	7 ns	Commercial	
GS72116AU-8	6 mm x 8 mm Fine Pitch BGA	8 ns	Commercial	
GS72116AU-10	6 mm x 8 mm Fine Pitch BGA	10 ns	Commercial	
GS72116AU-12	6 mm x 8 mm Fine Pitch BGA	12 ns	Commercial	
GS72116AU-7I	6 mm x 8 mm Fine Pitch BGA	7 ns	Industrial	
GS72116AU-8I	6 mm x 8 mm Fine Pitch BGA	8 ns	Industrial	
GS72116AU-10I	6 mm x 8 mm Fine Pitch BGA	10 ns	Industrial	
GS72116AU-12I	6 mm x 8 mm Fine Pitch BGA	12 ns	Industrial	

* Customers requiring delivery in Tape and Reel should add the character “T” to the end of the part number. For example: GS72116ATP-8T

2Mb Asynchronous Datasheet Revision History

Rev. Code: Old; New	Types of Changes Format or Content	Page #/Revisions/Reason
72116A_r1		• Creation of new datasheet
72116A_r1; 72116A_r1_01	Content	• Added 6 ns speed bin to entire document
72116A_r1_01; 72116A_r1_02	Content	• Updated all power numbers • Changed 6 mm x 10 mm FP_BGA package designator from U to X
72116A_r1_02; 72116A_r1_03	Content	• Updated Recommended Operating Conditions table on page 5 • Removed 15 ns bin • Changed FPBGA package from 6 x 10 to 6 x 8 (package U)
72116A_r1_03; 72116A_r1_04	Content	• Removed 6 ns speed bin from entire document • Added 7 ns speed bin to entire document
72116A_r1_04; 72116A_r1_05	Content	• Corrected title of 6 x 8 FPBGA mechanical drawing

